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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/043,946	01/11/2002	Jong Sik Paek	AMKOR-017A	6383

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EXAMINER
LEWIS, MONICA

ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/043,946	PAEK, JONG SIK
	Examiner	Art Unit
	Monica Lewis	2822

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11 and 19-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 19-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3 and 5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. This action is in response to the election filed August 13, 2002.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 3, 21 and 22 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is not clear what is meant by the following: a) "the conductive wires comprise first and second conductive wires" (See Claim 3); b) "respective ones" (See Claims 3 and 21). Claim 22 depends directly or indirectly from a rejected claim and are, therefore, also rejected under 35 U.S.C. 112, second paragraph for the reasons set above.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 9-11 and 19-22, as far as understood, are rejected under 35 U.S.C. 102(b) as being anticipated by Ball (U.S. Patent No. 5,689,135).

In regards to claim 1, Ball discloses the following:

a) a plurality of leads (See Figure 1 and Column 2 Lines 40-43);

b) first surface (See Figure 1);

c) second surface disposed in opposed relation to the first surface (See Figure 1);

d) a third surface disposed in opposed relation to the second surface, the first surface being oriented between the second and third surfaces (See Figure 1);

e) a first semiconductor die (14) defining opposed first and second surfaces and including a plurality of bond pads (38) disposed on the first surface thereof, the first surface of the first semiconductor die being attached to the second surface of each of the leads (See Figure 1);

f) a second semiconductor die (12) defining opposed first and second surfaces and including a plurality of bond pads (18) disposed on the second surface thereof, the first surface of the second semiconductor die being attached to the second surface of the first semiconductor die (See Figure 1);

g) a plurality of conductive connectors (26 and 36) electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads (See Figure 1); and

h) an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the conductive connectors (See Column 4 Lines 45-49).

In regards to claim 2, Ball discloses the following:

a) conductive connectors comprise conductive wires (See Figure 1).

In regards to claim 3, Ball discloses the following:

a) the conductive wires comprise first and second conductive wires (See Figure 1);

b) the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by respective ones of the first conductive wires (See Figure 1);

c) the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by respective ones of the second conductive wires (See Figure 1).

In regards to claim 9, Ball discloses the following:

a) the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion (See Figure 1).

In regards to claim 10, Ball discloses the following:

a) the first semiconductor die and the leads are oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact the second surface of any one of the leads (See Figure 1).

In regards to claim 11, Ball discloses the following:

a) the first semiconductor die defines a peripheral edge (See Figure 1);

b) the conductive connectors electrically connecting the bond pads of the first semiconductor die to the leads are oriented inwardly relative to the peripheral edge of the first semiconductor die (See Figure 1).

In regards to claim 19, Ball discloses the following:

a) a plurality of leads (See Figure 1 and Column 2 Lines 40-43);

b) a first semiconductor die including a plurality of bond pads disposed thereon, the first semiconductor die being attached to each of the leads (See Figure 1);

c) a second semiconductor die including a plurality of bond pads disposed thereon, the second semiconductor die being attached to the first semiconductor die (See Figure 1);

d) electrically connecting the bond pads of the first and second semiconductor dies to respective ones of the leads (See Figure 1); and

e) an encapsulating portion applied to and at least partially encapsulating the leads, the first and second semiconductor dies, and the electrical connection means (See Figure 1).

In regards to claim 20, Ball discloses the following:

a) the electrical connection means comprises conductive wires (See Figure 1).

In regards to claim 21, Ball discloses the following:

a) each of the leads defines opposed first and second surfaces and a third surface which is opposed to the second surface and oriented between the second and third surfaces (See Figure 1);

b) the bond pads of the first semiconductor die are electrically connected to respective ones of the first surfaces of the leads by respective ones of first conductive wires (See Figure 1); and

c) the bond pads of the second semiconductor die are electrically connected to respective ones of the second surfaces of the leads by respective ones of second conductive wires (See Figure 1).

In regards to claim 22, Ball discloses the following:

a) the encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion (See Figure 1).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 4-8 and 23-25 are rejected under 35 U.S.C. 103(a) as obvious over Ball (U.S. Patent No. 5,689,135) in view of Ball (U.S. Patent No. Re. 36,613).

In regards to claim 4, Ball fails to disclose the following:

a) a die paddle defining opposed top and bottom surfaces, the leads being disposed about the die paddle; and

b) the first surface of the first semiconductor die further being attached to the top surface of the die paddle.

However, Ball discloses a stacked device with a die paddle (14) (See Figure 2 and Column 3 Lines 19-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ball to include a die paddle as disclosed in Ball because it aids in providing support to the die stack.

In regards to claim 5, Ball discloses the following:

a) the first surface of the first semiconductor die is attached to the second surface of each of the leads (See Figure 1); and

b) the first surface of the second semiconductor die is attached to the second surface of the first semiconductor die by a second bonding means (See Figure 1).

In regards to claim 5, Ball fails to disclose the following:

a) a die paddle.

However, Ball discloses a stacked device with a die paddle (See Figure 2 and Column 3 Lines 19-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ball to include a die paddle as disclosed in Ball because it aids in providing support to the die stack.

In regards to claim 6, Ball discloses the following:

a) the leads is formed to have a lead thickness between the second and third surfaces thereof (See Figure 1).

In regards to claim 6, Ball fails to disclose the following:

a) the die paddle is formed to have a die paddle thickness; and

b) the die paddle thickness is substantially equal to the lead thickness.

However, Ball discloses a stacked device with a die paddle (See Figure 2 and Column 3 Lines 19-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ball to include a die paddle as disclosed in Ball because it aids in providing support to the die stack.

In regards to claim 7, Ball discloses the following:

a) encapsulating portion (See Figure 1).

In regards to claim 7, Ball fails to disclose the following:

a) the die paddle is exposed within the encapsulating portion.

However, Ball discloses a stacked device with a die paddle (See Figure 2 and Column 3 Lines 19-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ball to include a die paddle as disclosed in Ball because it aids in providing support to the die stack.

In regards to claim 8, Ball discloses the following:

a) encapsulating portion is applied to the leads such that the third surface of each of the leads is exposed within the encapsulating portion (See Figure 1).

In regards to claim 23, Ball fails to disclose the following:

a) a die paddle, the leads being disposed about the die paddle; and

b) the first semiconductor die being attached to the die paddle.

However, Ball discloses a stacked device with a die paddle (14) (See Figure 2 and Column 3 Lines 19-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ball to include a die paddle as disclosed in Ball because it aids in providing support to the die stack.

In regards to claim 24, Ball discloses the following:

a) encapsulating portion (See Figure 1).

In regards to claim 24, Ball fails to disclose the following:

a) the die paddle defines opposed top and bottom surfaces, with the first semiconductor die being attached to the top surface of the die paddle.

However, Ball discloses a stacked device with a die paddle (14) (See Figure 2 and Column 3 Lines 19-23). It would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the semiconductor device of Ball to include a die paddle as disclosed in Ball because it aids in providing support to the die stack.

In regards to claim 25, Ball discloses the following:

a) the first semiconductor die and the leads are oriented relative to each other such that each of the bond pads of the first semiconductor die is located between a respective pair of the leads so that the bond pads of the first semiconductor die do not contact any one of the leads (See Figure 1) .

Conclusion

9. The following prior art made of record and not relied upon is considered pertinent to applicant's disclosure: a) Rostoker (U.S. Patent No. 5,534,467) discloses a semiconductor package device; b) Sawai et al. (U.S. Patent No. 5,814,883) discloses a semiconductor device with a packaged with a semiconductor chip; c) Alagaratnam et al. (U.S. Patent No. 5,814,881) discloses a stacked integrated chip package; d) Lee (U.S. Patent No. 5,821,615) discloses a

semiconductor chip package having a clip type outlead; e) Mori (U.S. Patent No. 5,903,049) discloses a semiconductor module; f) Lenz (U.S. Patent No. 6,031,279) discloses a power semiconductor component; g) Lee et al. (U.S. Patent No. 6,087,722) discloses a multichip package; h) Fukui et al. (U.S. Patent No. 6,100,594) discloses a semiconductor device; i) Ishio et al. (U.S. Patent No. 6,118,184) discloses a semiconductor device sealed with a sealing resin; j) Juso et al. (U.S. Patent No. 6,181,002) discloses a semiconductor device having a plurality of chips; k) Corsis (U.S. Patent No. 6,303,984) discloses a lead frame including a tie bar; l) Ozawa et al. (U.S. Patent No. 6,316,838) discloses a semiconductor device; m) Kimura (U.S. Patent No. 2002/0011654) discloses a semiconductor device; and n) Shimoda (U.S. Patent No. 6,452,279) discloses a semiconductor device.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Monica Lewis whose telephone number is 703-305-3743. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 703-308-4905. The fax phone number for the organization where this application or proceeding is assigned is 703-308-7722 for regular and after final communications. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

ML
October 21, 2002

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